Claims

I claim:

1. A generator of a Viterbi decoder for generating a branch metric, comprising:

a linear feedback shift register for performing calculation on a specific primitive characteristic polynomial to generate a number sequence; and

a convolutional encoder, connected to the linear feedback shift register, for receiving and encoding the number sequence to generate the branch metric.

2. The generator of claim 1, wherein the linear feedback shift register comprises:

a number sequence generation circuit comprising an input end, a first output end and a second output end; and

a performing circuit, comprising a data input end and a data output end, used to perform calculation on the specific primitive characteristic polynomial;

wherein the first output end is connected to the data input end, the data output end is connected to the input end, and the second output end is connected to the convolutional encoder.

3. The generator of claim 2, wherein the number sequence generation circuit comprises:

N registers;

a NOR gate; and

an XOR gate;

wherein the number sequence generation circuit generates 2^N binary numbers.

4. The generator of claim 3, wherein each of the N registers comprises a D flip-flop.

5. The generator of claim 2, wherein the performing circuit comprises at least an XOR gate.

6. The generator of claim 3, wherein the convolutional encoder comprises at least an XOR gate.

7. A generator of a Viterbi decoder for generating a branch metric by selecting one of a plurality of primitive characteristic polynomials, comprising:

a selector;

a performing circuit set comprising a plurality of performing circuits, each of the plurality of performing circuits corresponding to one of the plurality of primitive characteristic polynomials, the performing circuit set outputting a plurality of calculation results to the selector;

a number sequence generation circuit, connected to the selector, for providing a number sequence to the selector; and

a convolutional encoder, connected to the number sequence generation circuit, for receiving the number sequence;

wherein the selector selects and returns one of the plurality of calculation results to the number sequence generation circuit, and the convolutional encoder encodes the number sequence to generate the branch metric.

8. The generator of claim 7, wherein the selector comprises:

a selection input end for inputting a selection signal;

a multiplexer for receiving the plurality of calculation results and the selection signal; and

a select logic gate for receiving the selection signal.

9. The generator of claim 7, wherein the number sequence generation circuit comprises:

N registers;

a NOR gate; and

an XOR gate;

wherein the number sequence generation circuit generates 2^N binary numbers.

10. The generator of claim 9, wherein each of the N registers comprises a D flip-flop.

11. The generator of claim 7, wherein the performing circuit comprises at least an XOR gate.

12. The generator of claim 7, wherein the convolutional encoder comprises at least an XOR gate.